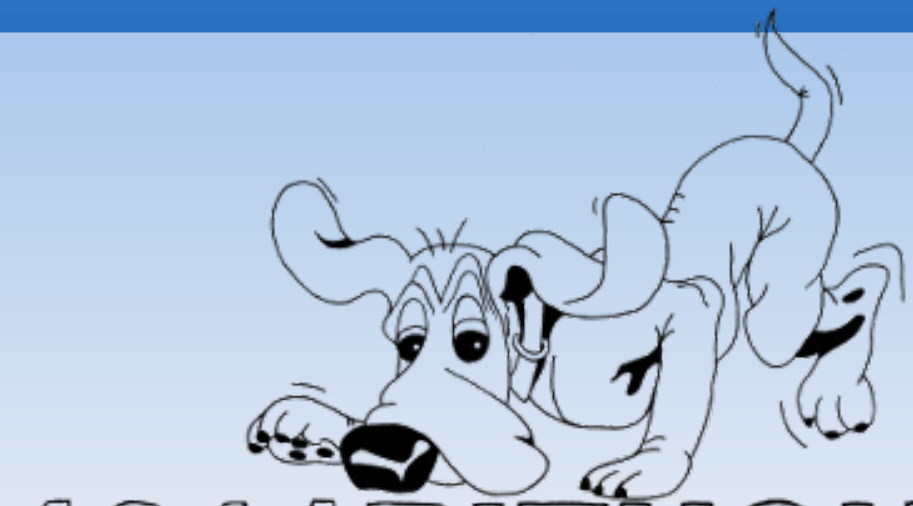
Digilent Design Contest 2011



1011BITHOUND1101

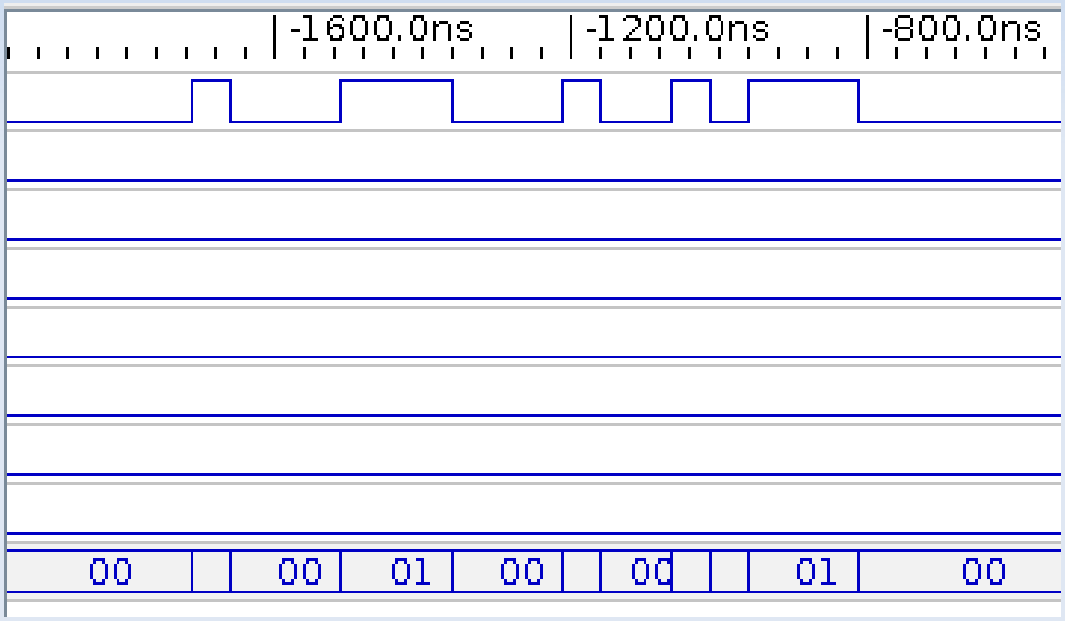
An FPGA based Logic Analyzer

Lukas Schrittwieser
Mario Mauerer

September 2011

Motivation

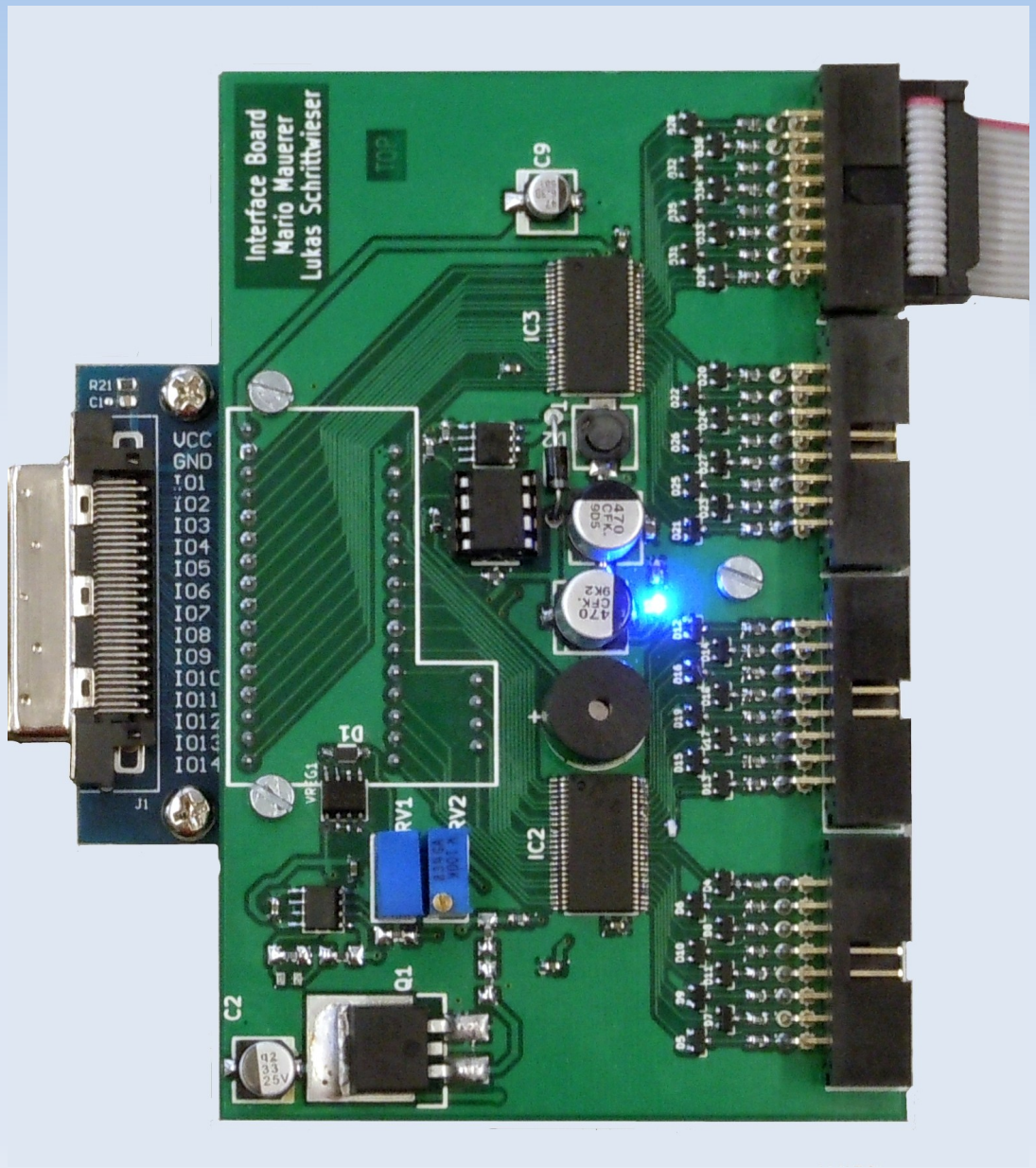
Build a easy to use Logic Analyzer for inspecting and debugging digital circuits



Project Goals

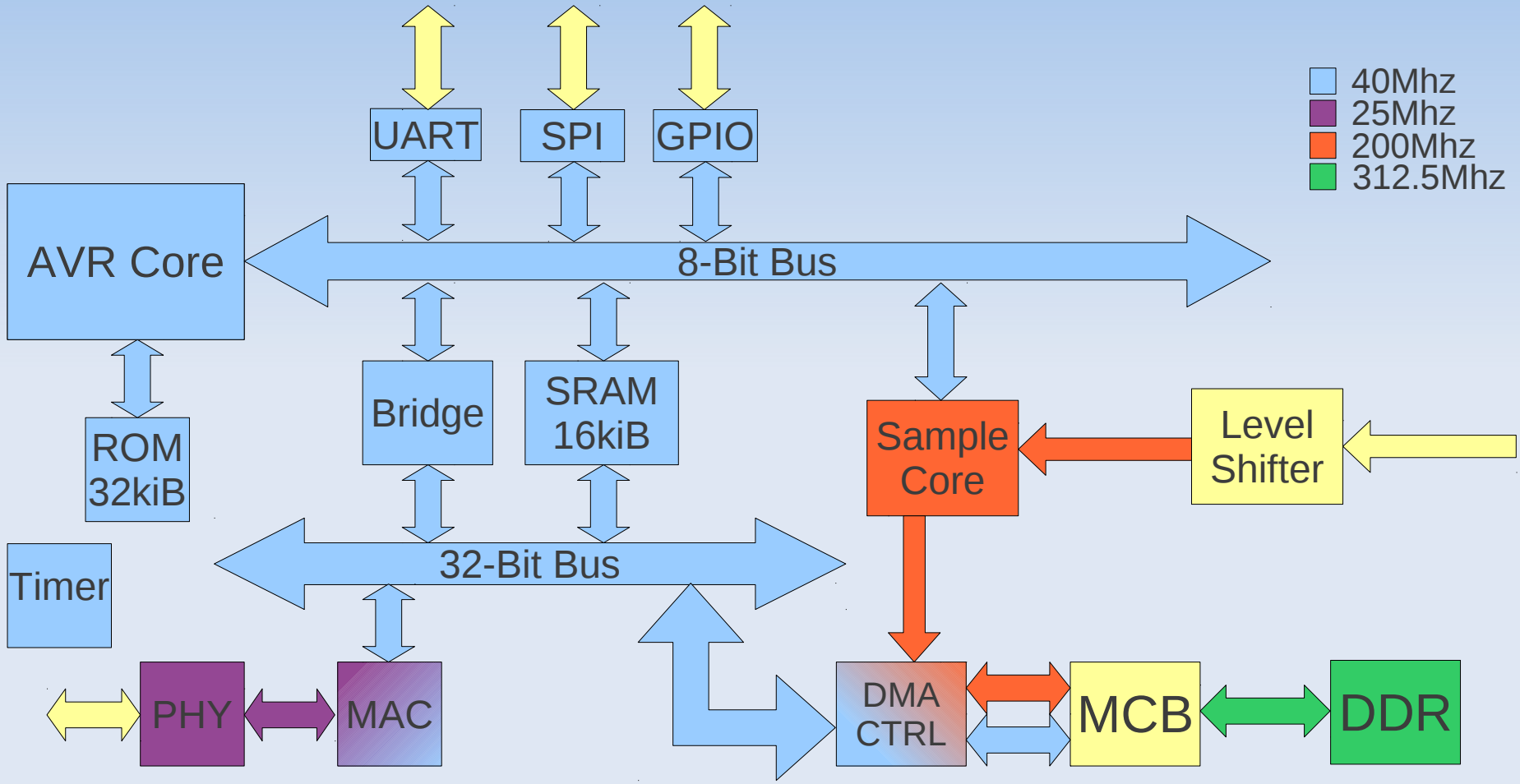
- Basis: ”SUMP” logic analyzer
- Atlys Spartan-6 FPGA evaluation board
- 128MiB DDR2 sample memory
- 400MHz sampling frequency
- Ethernet instead of UART
- Build an Interface Board

Interface Board



- Probes
- Level Shifters
- Overvoltage-Protection

FPGA Design


40Mhz
25Mhz
200Mhz
312.5Mhz
UART
SPI
GPIO
AVR Core
8-Bit Bus
ROM
32kiB
Bridge
SRAM
16kiB
Sample
Core
Level
Shifter
Timer
32-Bit Bus
PHY
MAC
DMA
CTRL
MCB
DDR

Firmware

- Entire project in C
- TCP/IP Stack: uIP (open source)
- TCP stream for control
- UDP for sampled data
  - Less overhead than TCP
  - > 7MByte/s
- UDP advertisement broadcasts
  - Client can find LA in the network

Software

- Adapted from SUMP
  - Written in Java → platform independant
- Ethernet Interface
  - UDP Broadcast reception
  - Reordering and Retransmission for Datagrams
- New GUI Features
  - New powerful Trigger configuration
  - Markers to flag interesting sections
  - 'Next Edge' & 'Prev Edge'
  - Rendering speedup

Conclusion

- Potential for improvements
  - Pattern search
  - More protocol decoders (UART, USB, …)
  - Gigabit Ethernet

Demo